Amendments to the Claims:

Please replace all prior versions, and listings of claims in the application with the following listing of claims.

Listing of claims

1. (Currently Amended) Apparatus for use in a computer system comprising:

an open-ended ~~a~~ pipeline bus architecture, in which data traverses the bus architecture over a plurality of system clock cycles; and

a plurality of modules adapted for selective connection to the bus architecture, [[;]] wherein the bus architecture comprises:

a plurality of bus connection units; and

a plurality of bus portions arranged in open-ended series, each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus connection unit, each of the bus connection units including multiplexer circuitry for selectively connecting a module to the bus architecture, wherein

the modules are connected to the bus architecture only by way of the bus connection units and in response to operation of the multiplexer circuitry.

2. (Previously Presented) Apparatus as claimed in claim 1, wherein each bus connection unit includes output circuitry connected to the bus portions to which the unit is connected, the output circuitry being tailored to optimize the signal characteristics for the physical length of the bus portions concerned.

3. (Previously Presented) Apparatus as claimed in claim 1, wherein the bus portions are all equal in physical length.

4. (Previously Presented) Apparatus as claimed in claim 1, wherein the pipeline bus architecture comprises a primary pipelined bus and a secondary pipelined bus, the primary and secondary buses being interconnected by an interface, a first plurality of modules connected to the primary bus by means of respective said bus connection units, and a second plurality of modules connected to the secondary bus by means of respective said bus connection units.

5. (Original) Apparatus as claimed in claim 1, wherein a central arbitration unit arbitrates between the modules in order to grant access to the bus architecture.

6. (Original) Apparatus as claimed claim 5, wherein the pipelined bus architecture comprises a primary pipelined bus and a secondary pipelined bus, the primary and secondary buses interconnected by an interface, a first plurality of modules connected to the primary bus by means of respective said bus connection units, and a second plurality of modules connected to the secondary bus by means of respective said bus connection units.

7. (Original) Apparatus as claimed in claim 4, wherein the first plurality of modules are latency intolerant and the second plurality of modules are latency tolerant.

8. (Previously Presented) Apparatus as claimed in claim 4, wherein the primary bus has a length of one pipeline stage, said length being the bus length traveled by a data pulse in a single system clock cycle.

9. (Original) Apparatus as claimed in claim 1, wherein transactions involving data in excess of a predetermined size are split into a plurality of data packets of fixed size, said packets being independently arbitrated.

10. (Previously Presented) Apparatus as claimed in claim 1 wherein said bus architecture comprises separate read, write and transaction buses.

11. (Original) Apparatus as claimed in claim 1, wherein the bus architecture has a width sufficient to permit read and write request transactions to alternate in successive system clock cycles.

12. (Original) A computer system comprising apparatus as claimed in claim 1.

12. (Currently Amended) A computer system comprising ~~apparatus as claimed in claim 1~~:

an open-ended pipeline bus architecture, in which data traverses the bus architecture over a plurality of system clock cycles; and

a plurality of modules adapted for selective connection to the bus architecture, wherein the bus architecture comprises:

a plurality of bus connection units; and

a plurality of bus portions arranged in open-ended series, each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus connection unit, each of the bus connection units including multiplexer circuitry for selectively connecting a module to the bus architecture, wherein

the modules are connected to the bus architecture only by way of the bus connection units and in response to operation of the multiplexer circuitry.

13. (New) An integrated processing device comprising:

an open-ended pipeline bus architecture, in which data traverses the bus architecture over a plurality of system clock cycles; and

a plurality of modules adapted for selective connection to the bus architecture;

wherein the bus architecture comprises:

a plurality of bus connection units; and

a plurality of bus portions arranged in an open-ended series, each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus connection unit,

each of the bus connection units including multiplexer circuitry for selectively connecting a module to the bus architecture,

wherein the modules are connected to the bus architecture only by way of the bus connection units and in response to operation of the multiplexer circuitry.

14. (New) An integrated processing device as claimed in claim 13, wherein each bus connection unit includes output circuitry connected to the bus portions to which the unit is connected, the output circuitry being tailored to optimise the signal characteristics for the physical length of the bus portions concerned.

15. (New) An integrated processing device as claimed in claim 13, wherein the bus portions are all equal in physical length.

16. (New) An integrated processing device as claimed in claim 13, wherein the pipeline bus architecture comprises a primary pipelined bus and a secondary pipelined bus, the primary and secondary buses being interconnected by an interface, a first plurality of modules connected to the primary bus by means of respective said bus connection units, and a second plurality of modules connected to the secondary bus by means of respective said bus connection units.

17. (New) An integrated processing device as claimed in claim 13, wherein a central arbitration unit arbitrates between the modules in order to grant access to the bus architecture.

18. (New) An integrated processing device as claimed in claim 17, wherein the pipelined bus architecture comprises a primary pipelined bus and a secondary pipelined bus, the primary and secondary buses interconnected by an interface, a first plurality of modules connected to the primary bus by means of respective said bus connection units, and a second

plurality of modules connected to the secondary bus by means of respective said bus connection units.

19. (New) An integrated processing device as claimed in claim 16, wherein the first plurality of modules are latency intolerant and the second plurality of modules are latency tolerant.

20. (New) An integrated processing device as claimed in claim 4, wherein the primary bus has a length of one pipeline stage, said length being the bus length travelled by a data pulse in a single system clock cycle.

21. (New) An integrated processing device as claimed in claim 13, wherein transactions involving data in excess of a predetermined size are split into a plurality of data packets of fixed size, said packets being independently arbitrated.

22. (New) An integrated processing device as claimed in claim 13, wherein said bus architecture comprises separate read, write and transaction buses.

23. (New) An integrated processing device as claimed in claim 13, wherein the bus architecture has a width sufficient to permit read and write request transactions to alternate in successive system clock cycles.